The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

Sub B1 1. In an inverter circuit having at least one pair of alternately conducting transistors in circuit with a DC voltage input and being operable to provide an AC voltage output, the improvement comprising:

means comprising a series-connected combination of an inductor and a capacitor in circuit with the transistors and energized upon alternate conduction thereof; and

means for providing drive current to the transistors to control the inversion frequency thereof to be higher than the natural resonant frequency of the inductor and capacitor combination.

2. The inverter circuit of claim 1 wherein the drive current means is in circuit with the inductor and comprises at least one saturable inductor means operable to provide drive current to the transistors to effect inverter self-oscillation, the conduction period of each transistor being determined by the saturation time of the saturable inductor means.

3. The inverter circuit of claim 2 wherein the drive means comprises means for supplying reverse bias to the conducting transistor upon saturation of the saturable inductor means.

4. The inverter circuit of claim 3 wherein the reverse bias means comprises a Zener diode.

5. The inverter circuit of claim 3 wherein each transistor comprises a base, an emitter and a collector, and wherein the level of reverse bias for each transistor is determined by the reverse breakdown voltage of the base-emitter junction thereof.

6. The inverter circuit of claim 2 wherein the transistors are connected in series across the DC voltage input.

7. The inverter circuit of claim 6 wherein each of the transistors comprises a base, an emitter and a collector; the inverter circuit further comprising a second capacitor connected across the collector-emitter terminals of at least one of the transistors, the second capacitor being operable to restrain the rate of voltage change across said terminals.

8. The inverter circuit of claim 1 wherein each of the transistors comprises a base, an emitter and a collector, and wherein the transistors are connected in parallel; the inverter circuit comprising a second capacitor connected between the collectors of the transistors, the second capacitor being operable to restrain the rate of voltage change on the collectors.

9. The inverter circuit of claim 1 and a shunt diode connected across the collector-emitter terminals of each transistor.

10. The inverter circuit of claim 1 and a load connected in circuit with the inductor and the capacitor, the load being operable to limit the voltages developed across the inductor and the capacitor to non-destructive levels.

~~11. The inverter circuit~~ of claim 10 wherein the load comprises a gas discharge lamp.

12. The inverter circuit of claim 11 wherein the lamp and the capacitor constitute a self-contained unit.

13. The inverter circuit of claim 1 and a fluorescent lamp having a pair of cathodes in circuit with the inductor and the capacitor, and wherein the inductor comprises a pair of magnetically-coupled auxiliary windings for electrically ~~heating the cathodes.~~

14. In an inverter circuit having at least one pair of alternately conducting transistors in circuit with a DC voltage input and being operable to provide an AC voltage output, the improvement comprising:

means comprising a series-connected combination of an inductor and a capacitor in circuit with the transistors and energized upon alternate conduction thereof; and

means for providing drive current to the transistors to control each conduction period thereof to be shorter in duration than one quarter of the full period corresponding to the natural resonant frequency of the inductor and capacitor combination.

15. The inverter circuit of claim 14 wherein the drive current means is in circuit with the inductor and comprises at least one saturable inductor means operable to provide drive current to the transistors to effect inverter self-oscillation, the conduction period of each transistor being determined by the saturation time of the saturable inductor means.

16. The inverter circuit of claim 15 wherein the drive means comprises means for supplying reverse bias to the conducting transistor upon saturation of the saturable inductor means.

17. The inverter circuit of claim 14 and a shunt diode connected across the collector-emitter terminals of each transistor.

18. The inverter circuit of claim 14 wherein the transistors are connected in series across the DC voltage input.

19. The inverter circuit of claim 18 wherein each of the transistors comprises a base, an emitter and a collector; the inverter circuit further comprising a second capacitor connected across the emitter-collector terminals of at least one of the transistors, the second capacitor being operable to restrain the rate of voltage change across said terminals.

20. The inverter circuit of claim 14 and a load connected in circuit with the inductor and the capacitor, the load being operable to limit the voltages developed across the inductor and the capacitor to non-destructive levels.

~~21.~~ The inverter circuit of claim 20 wherein the load comprises a gas discharge lamp.

22. The inverter circuit of claim 14 wherein the drive current means is in circuit with the inductor and is operable to provide drive current only after the current through the inductor has diminished to zero.

23. The inverter circuit of claim 14 wherein the drive current means is in circuit with the inductor and is operable to terminate the drive current before the current through the inductor has reached its maximum amplitude.

~~24. In an inverter circuit~~ having at least one periodically conducting transistor in circuit with a supply of unidirectional voltage and being operable to provide an AC voltage output, the improvement comprising:

means comprising a series-connected combination of an inductor and a capacitor in circuit with the transistor and energized upon periodic conduction thereof; and

a fluorescent lamp in circuit with the inductor-capacitor combination;

whereby the fluorescent lamp is operable to limit the voltages developed across the inductor and capacitor to ~~non-destructive levels.~~

~~25. A power supply for providing~~ a voltage output, comprising:

rectifier means being optionally connectable to a first AC voltage input; and

voltage doubler and rectifier means being optionally connectable to a second AC voltage input having an amplitude that is approximately one-half the amplitude of the first AC voltage input;

whereby the rectifier means and the voltage doubler and rectifier means are selectively operable to provide substantially the same magnitude of DC voltage output.

26. The power supply of claim 25 and switching means for alternative connection of the rectifier means and the voltage doubler and rectifier means to the first and second AC input voltages, respectively.

27. In an inverter circuit connected to a DC voltage input and being operable to provide an AC voltage output, the improvement comprising:

rectifier means being optionally connectable to a first AC voltage input; and

voltage doubler and rectifier means being optionally connectable to a second AC voltage input having an amplitude approximately one-half the amplitude of the first AC voltage input;

whereby the rectifier means and the voltage doubler and rectifier means are selectively operable to provide substantially the same magnitude of DC voltage input ~~to the inverter.~~

~~28. The inverter circuit~~ of claim 27 wherein the rectifier means comprises a bridge rectifier having four diodes and wherein the voltage doubler and rectifier means comprises at least two of said diodes.

29. The inverter circuit of claim 27 and switching means for alternative connection of the rectifier means and the voltage doubler and rectifier means to the first and second AC input voltages, respectively.

30. The inverter circuit of claim 27 and a pair of alternately conducting transistors connected in series across the DC voltage.

31. The inverter circuit of claim 27 wherein the AC voltage input comprises two power leads and wherein the voltage doubler and rectifier means provides a direct electrical connection between one of the power lines and the ~~inverter~~ circuit.

32. In an inverter circuit having a pair of alternately conducting transistors connected in series across a DC voltage supply and being operable to provide an AC voltage output, the improvement comprising:

means providing an AC input voltage on two power leads;

an inductor means in circuit with the common connection of the transistors;

a load in circuit with the inductor means; and

power supply means in circuit with the AC input voltage and being operable to provide the DC voltage supply to the inverter, the power supply means providing a direct electrical connection between one of the power leads and the inductor means.

33. A self-ballasted gas discharge lamp unit comprising:

an inverter having at least one periodically conducting transistor in circuit with a DC voltage input and being operable to provide an AC voltage output;

the inverter comprising a tank circuit having an inductor and a capacitor energized upon periodic transistor conduction;

the inverter further comprising means for providing transistor drive current to control the inversion frequency thereof to be at least equal to the natural resonant frequency of the tank circuit.

34. The lamp unit of claim 33 wherein the drive current means comprises at least one saturable inductor means operable to provide transistor drive current to effect inverter self-oscillation, the transistor conduction period being determined by the saturable inductor means saturation time.

35. ~~A self-ballasted~~ gas discharge lamp unit comprising:

a gas discharge lamp having a pair of electrodes;

a base secured to the lamp and containing an AC power supply for providing a voltage of a magnitude sufficient for instant starting of the lamp;

the power supply comprising an inverter in circuit with a DC input voltage and having at least one periodically conducting transistor and means comprising an inductor and a capacitor in circuit therewith to be energized upon periodic transistor conduction, the inductor and capacitor being in circuit with the lamp electrodes.

36. The self-ballasted gas discharge lamp unit of claim 35 wherein the gas discharge lamp is a fluorescent lamp.

37. The self-ballasted lamp unit of claim 35 wherein the inverter comprises two alternately conducting transistors connected in series across the DC voltage.

38. The lamp unit of claim 35 and means for providing transistor drive current to control the frequency of the transistor conduction to be at least equal to the natural resonant frequency of the inductor and capacitor combination.

39. The lamp unit of claim 38 wherein the drive current means comprises at least one saturable inductor means, the transistor conduction period being determined by ~~the~~ saturation time of the ~~saturable inductor means.~~

~~40. The lamp unit of~~ claim 35 wherein the base is adapted for screw-in insertion into a conventional Edison-type socket at which a relatively low frequency AC voltage is available, the power supply further comprising means for rectifying the low frequency AC voltage for providing the DC input voltage to the inverter circuit.

41. The lamp unit of claim 35 and a starting aid electrode in proximity with the lamp.

42. The lamp unit of claim 35 wherein the inductance value of the inductor is manually variable whereby to effect illumination of the lamp at adjustable levels.

43. A power supply operable to energize a gas discharge lamp at adjustable illumination levels, comprising:

an inverter circuit having at least one periodically conducting transistor in circuit with a DC voltage input and being operable to provide an AC voltage output to the lamp;

frequency dependent impedance means in circuit with the AC voltage output and the lamp; and

means for adjustably controlling the transistor inversion frequency and hence the magnitude of the AC current supplied to the lamp.

44. The power supply of claim 43 wherein the controlling means comprises a saturable inductor means.

45. The power supply of claim 44 wherein the saturable inductor means has an adjustable saturation flux density for control of its saturation time.

46. In an inverter circuit having at least one periodically conducting transistor in circuit with a DC voltage input and being operable to provide an AC voltage output, the improvement comprising:

means comprising at least one saturable inductor for providing transistor drive current to control the conduction frequency thereof; and

means for controllably heating the saturable inductor whereby to correspondingly decrease the saturation flux limit and the saturation time thereof to increase the transistor inversion frequency.

47. The inverter circuit of claim 46 and means for adjustably controlling the heating means.

48. The inverter circuit of claim 46 wherein the transistor dissipates heat upon periodic conduction thereof and the heating means is operable to provide heat from the transistor to the saturable inductor.

49. The inverter circuit of claim 46 wherein the heating means is electrically powered, and wherein the inverter circuit further comprises a frequency dependent impedance means in circuit with the output and means for supplying power to the heating means in accordance with the level of the output whereby to effect feedback regulation thereof.

50. In a half-bridge inverter circuit connected to a DC voltage input and being operable to provide an AC voltage output, the inverter circuit comprising a pair of alternately conducting transistors connected in series across the DC voltage input, the improvement comprising:

current feedback means in circuit with the output and comprising at least one saturable inductor operable to provide drive current to the transistors to effect alternate conduction thereof; and

a load in circuit with the transistors and having an inductance of value sufficient to effect periodic energy storage for self-sustained transistor inversion.

51. In a half-bridge inverter circuit connected to a DC voltage input and being operable to provide an AC voltage output, the inverter circuit comprising a pair of alternately conducting transistors connected in series across the DC voltage input, the improvement comprising:

a load in circuit with the transistors and being operable to effect periodic energy storage; and

a shunt diode connected in circuit with each transistor to provide a path of relatively low impedance to the DC voltage input for energy periodically stored in the load.

52. In a half-bridge inverter circuit connected to a DC voltage input and being operable to provide an AC voltage output, the inverter circuit comprising a pair of alternately conducting transistors connected in series across the DC voltage input each transistor having base, emitter and collector terminals, the improvement comprising a capacitor connected between the collector and emitter terminals of at least one of the transistors, the capacitor being operable to restrain the rate of rise of voltage across said terminals.

53. In a half-bridge inverter circuit connected to a DC voltage input and being operable to provide an AC voltage output, the inverter circuit comprising a pair of alternately conducting transistors connected in series across the DC voltage input, the improvement comprising:

current feedback means in circuit with the output and comprising at least one saturable inductor operable to provide drive current to the transistors to effect alternate conduction thereof; and

means for supplying reverse bias to the conducting transistor upon saturation of the saturable inductor.

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